



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,668	03/29/2004	Kenji Ichikawa	SAT 200	1142
23995	7590	06/10/2005	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005			LE, THAO X	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/810,668	ICHIKAWA, KENJI	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 29 March 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16-30 is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 March 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>03/29/05</u>  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Specification***

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: a drawing to show 'a second-conductivity-type MOS protection transistor having a drain connected to the drain of said second-conductivity-type MOS output transistor, a source connected to a source of said second-conductivity-type MOS output transistor, and a gate connected to a first-conductivity-type layer under a gate of said second-conductivity-type MOS output transistor'.

### ***Drawings***

3. Figures 6, 7(a-b) and 8(a-b) should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.  
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (APA).

Regarding claim, APA discloses in fig. 6 a semiconductor apparatus, which protects a first-conductivity-type MOS output transistor 61, specification page 1 line 17, against a surge entering through an output electrode 64, spec page 1 line 16, connected to a drain of said first-conductivity-type MOS output transistor 61, said apparatus comprising: a first-conductivity-type MOS protection transistor 60, spec page 1 line 17, having a drain connected to the drain of said first-conductivity-type MOS output transistor 61, a source connected to a source of said first-conductivity-type MOS output transistor 61, and a gate connected to a second-conductivity-type layer (p substrate) under a gate of said first-conductivity-type MOS output transistor 61.

The gate of protection transistor 60 is connecting to the source of the output transistor 61 that also is connecting the player 72, fig. 6 spec page 2 line 11.

Art Unit: 2814

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 4-5 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6646840 to Sugerman et al.

Regarding claim 1, Sugerman discloses in fig. 4-5 a semiconductor apparatus, which protects a first-conductivity-type MOS output transistor m10, column 5 line 51, against a surge entering through an output electrode 20, column 5 line 40, connected to a drain of said first-conductivity-type MOS output transistor m10, said apparatus comprising: a first-conductivity-type MOS protection transistor m11, column 5 line 52, having a drain connected to the drain of said first-conductivity-type MOS output transistor M11, a source connected to a source of said first-conductivity-type MOS output transistor m10, and a gate 170, column 6 line 32, connected to a second-conductivity-type layer 140, column 6 line 22, under a gate 160, column 6 line 30 of said first-conductivity-type MOS output transistor m10.

Regarding claim 4, Sugerman discloses the semiconductor apparatus according to claim 1 wherein the gate 170 of said first-conductivity-type MOS protection transistor m11 is connected by an electrode wiring to said second-conductivity-type layer 140 under the gate 160 of said first-conductivity-type MOS output transistor m10, fig. 5.

Regarding claim 5, Sugerman discloses the semiconductor apparatus according to claim 1, wherein the drain of said first-conductivity-type MOS protection transistor m11 is formed closer to the output electrode 20 than the drain of said first-conductivity-type MOS output transistor m10, fig. 4.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 2-3, 6-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6646840 to Sugerman et al. in view of US 5610790 to Staab et al.

Regarding claims 2, 7, 11 and 14, Sugerman does not disclose the semiconductor apparatus according to claim 1, wherein said first-conductivity-type MOS output transistor m10 and said first-conductivity-type MOS protection transistor m11 are of an SOI structure.

However, Staab discloses the semiconductor apparatus in fig. 7-8a a protection circuit 700 comprises first-conductivity-type MOS output transistor 722, column 6 line 67, and said first-conductivity-type MOS protection transistor 716, column 7 line 4, are of an SOI structure, fig 8a column 6 line 45. At the time the invention was made; it would have been obvious to one of ordinary skill in the art

to use the SOI substrate teaching of Staab with Sugerman's device, because it would have increased the device speed as taught by Staab, see abstract.

Regarding claim 3, 8, 12, and 15, Sugerman discloses the semiconductor apparatus according to claim 2, comprising: a second-conductivity-type area 210, column7 line 5, connected to said second-conductivity-type layer 140 under the gate of said first-conductivity-type MOS output transistor m10, wherein the gate 160 of said first-conductivity-type MOS protection transistor m10 is connected via said second-conductivity-type area 210 to said second-conductivity-type layer 140 under the gate of said first-conductivity-type MOS output transistor m10.

Regarding claim 6, Sugerman does not disclose the semiconductor apparatus according to claim 1, wherein said first-conductivity-type MOS protection transistor is higher in electrostatic destruction withstand voltage than said first-conductivity-type MOS output transistor m10.

However, Sugerman discloses the structure in fig. 4-5 is substantially or identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 9 and 13 Sugerman discloses the semiconductor apparatus according to claim 6 wherein the gate 170 of said first-conductivity-type MOS

protection transistor m11 is connected by an electrode wiring to said second-conductivity-type layer 140 under the gate 160 of said first-conductivity-type MOS output transistor m10.

Regarding claim 10, Sugerman discloses the semiconductor apparatus according to claim 6, wherein the drain of said first-conductivity-type MOS protection transistor m11 is formed closer to the output electrode 20 than the drain of said first-conductivity-type MOS output transistor m10, fig. 4.

#### ***Allowable Subject Matter***

10. Claims 16-30 are allowed because the prior art of record neither anticipated nor rendered obvious all the limitation of the base claim 16 including 'a second-conductivity-type MOS protection transistor 62 having a drain connected to the drain of said second-conductivity-type MOS output transistor 63, a source connected to a source of said second-conductivity-type MOS output transistor, and a gate connected to a first-conductivity-type layer under a gate of said second-conductivity-type MOS output transistor'.

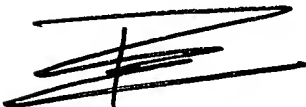
#### ***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.



If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le  
Patent Examiner  
07 June 2005